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Matrix Converter Based Multiport Power Electronic Transformer for Hybrid Distribution System

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ABSTRACT—Matrix converter offers many advantages as compared to dc link based VSI converter topologies. It has all the advantages of an ac-dc-ac conversion system while the bulky DC link capacitor for maintaining the dc link voltage is eliminated. This paper proposes matrix converter based multiport power electronic transformer (PET) which has one AC input port, one Medium level DC Voltage (MVDC) port and one Low DC Voltage (LVDC) port. Two phase shifted matrix converter stages are cascaded to obtain an interleaved output to minimize line frequency ripples. The frequency of operation of the matrix converter is 5 kHz, and hence the isolation transformer used in the LVDC circuit is smaller. Further the reactive elements used in the low pass filter of the MVDC circuit will be smaller because of the medium frequency operation of the matrix converter stages. The MVDC is obtained by rectification of the cascaded outputs of the two matrix converters. For obtaining LVDC the cascaded output is fed to a medium frequency step down transformer followed by rectification and a buck converter. The MVDC output is maintained by controlling the matrix converter switching while the LVDC output is maintained by controlling the switching of the buck converter. This arrangement ensures perfect decoupling between MVDC and LVDC outputs. A simple PI controller is used for the matrix converter while Sliding Mode Control (SMC) is used for the buck converter. The circuit has been extensively simulated in MATLAB - Simulink and the simulation results match with the analytical results.

Keywords—Power electronic transformer, Hybrid AC/DC grid, SMC, Medium- frequency transformer (MFT), Matrix converter.

I. INTRODUCTION

AC-AC conversion systems take fixed frequency with fixed ac voltage as input and provide variable ac frequency with variable voltage output. This can be achieved by two methods: 1) direct method and 2) Indirect method. The indirect method is the most commonly used for the ac-ac power conversion, which consists of a inverter at the load side and an rectifier at the supply side. Such an arrangement would require an energy storage element like an inductor or a capacitor in the intermediate DC link. These elements make the converter bulky and lead to poor response times. The second method is direct conversion wherein the DC link is eliminated and the intermediate stage can be considered as a pseudo dc link. The desirable features for any power frequency changer are 1) Generation of load voltage with capricious amplitude and frequency 2) Simple and compact power circuit 3) Sinusoidal input and output currents 4) Regeneration capability 5) Operation with unity power factor for any load. conventional cyclo-converters offer AC-AC conversion but the output frequency range is limited to the input supply frequency. The matrix converters on the other hand, offer flexibility in the range of output frequency as the output frequency can exceed the input frequency. Thus, the matrix converter has all desirable features of an AC-AC conversion system. The matrix-converter provides direct ACAC conversion without any bulky reactive elements. It system consists of bidirectional switches which allow any input phase to be connected to any output phase. Gyugyi first proposed the topology [1] - [4]. The power system can be consist of in three parts: power distribution, power transmission and power generation. Hybrid microgrids will have both AC and DC distribution systems and usually get integrated with main grid at distribution level. Usually in hybrid microgrids we may have a dc grid of low voltage, a dc grid of medium voltage and an ac system of single phase, 50 Hz, 230 V or three phase , 50 Hz, 415 V. In order to obtain the required LVDC levels 50 Hz input needs to be stepped

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down, which requires a 50 Hz bulky transformer. However, if a matrix converter is used with higher carrier frequencies, the transformer size will be significantly reduced. Such a conversion is realised in [2] using multi-level modular converter (MMC). Such a conversion system with one ac input port and two DC output ports of different levels can be termed as a power electronic transformer (PET) [3], [5] . PETs have three distinct circuits i.e. AC to DC, DC to DC and DC to AC circuits . Use of high/medium frequency results in reduction of transformer size [6]. These converters increase the frequency of operation to a higher level and maintain the required voltage levels at the output ports [7]. The PETs reported in literature a) Two stage PET b) three stage PET c) four-stage PET. The PETs of [8] and [10] have a simple configuration and reduced losses. However, there is no provision multiple DC outputs . Converters in belong to category c) listed above. They use MMCs as basic modules to be configured to get the desired voltage levels. Further they have input-series-output-parallel (ISOP) configuration for DC-DC conversion. In [12], dual active bridge (DAB) converters and energy storage systems are directly connected with half-bridge (HB) submodules (SMs) in MMC-based PETs. All of these MMC-based PETs have MVDC and LVDC ports. However, these MMC-based PETs have four power conversion stages, causing the complex structure leading to low efficiency, and low power density of PETs [9]. For example, in [9] the four power conversion stages from MVAC port to LVAC port include MVACMVDC stage, MVDC-LVAC stage, LVAC-LVDC stage and LVDC-LVAC stage. In the conversion stages are, from MVAC port to LVAC port are MVAC-LVDC stage, LVDCLVAC stage, LVAC-LVDC stage and LVDC-LVAC stage, respectively. In this paper instead of using MMC based PET a matrix converter-based PET is proposed. In the proposed PET, two cascaded single phase matrix converters, operating with phase difference of 900 , are used. This configuration uses a total of 16 switches. The modulation strategy can be suitably selected depending on the desired output levels. Whereas, in [12], multiple MMC stages need to be added for different levels of voltages.

II. SYSTEM DESCRIPTION

- **Block Diagram**

The block diagram of the proposed PET is shown in Fig. 1. In the block diagram there are two single phase, 50 Hz, 230 V inputs with phase difference of 900 between them, feeding the two cascaded matrix converters. Both the matrix converters are operated at carrier frequency of 5 kHz. The interleaved cascaded output of the two stages has a fundamental frequency of 5 kHz. This is given to a medium frequency transformer and parallelly to a diode rectification stage. The low pass filter used in the diode rectification stage has cut off frequency of 4.5 kHz which results in smaller reactive elements. The output of this stage is desired MVDC of 200 V. The matrix converters are operated with symmetrical multiple pulses in each half cycle of the respective input voltages. The PWM strategy of the matrix converters ensures that the MVDC is maintained at 200 V for all possible loads on the MVDC port. The medium frequency transformer output is fed to a buck converter which is operated such that the output LVDC level is maintained at 12 V for all possible loads on the LVDC port. Overall control strategy is such that LVDC and MVDC outputs are independently controlled which effectively leads to complete decoupling between the two outputs as explained in subsequent sections.

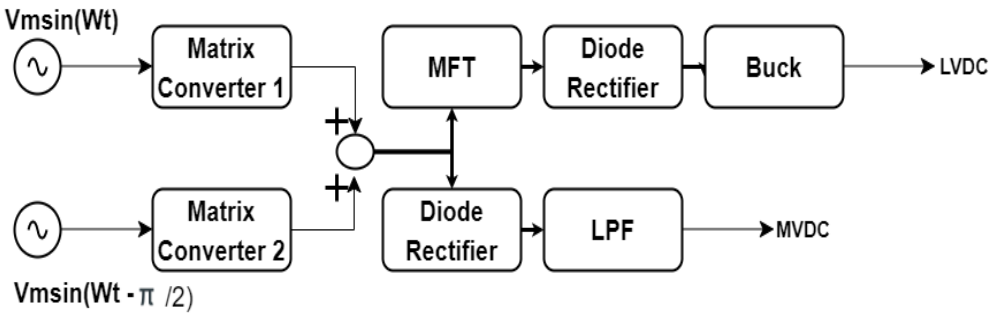

Fig. 1. Block diagram of the proposed PET

- **Circuit Diagram**

The detailed circuit diagram is shown in Fig. 2.The proposed PET consists of two matrix converters whose outputs are cascaded to obtain the intermediate medium frequency output. The input to the first matrix converter is $230\sqrt{2}\sin(\omega t)$ and input

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of second matrix converter is $230\sqrt{2}\sin(\omega t - \pi/2)$. Each matrix converter consists of four bidirectional switches. The switching strategy of cascaded matrix converter is described in section III.

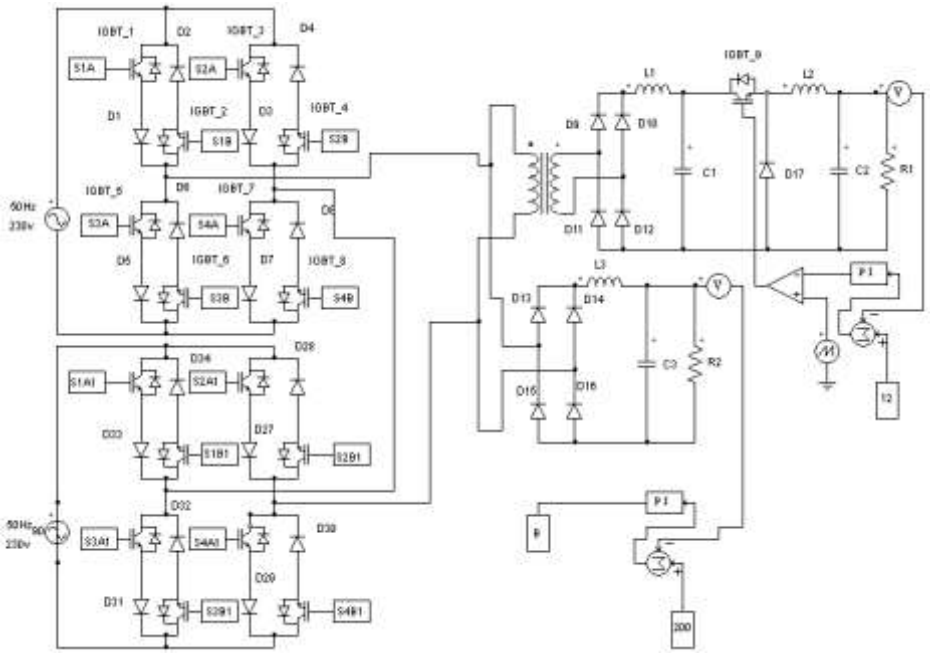
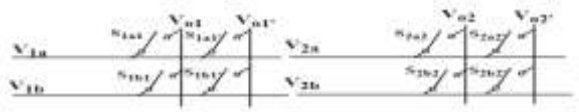


Fig. 2. Circuit diagram of the proposed PET

III. MATRIX CONVERTER

Fig. 3 shows the configuration of the individual matrix converters and all notations of circuit variables and generic switches used for analysis are indicated in the figure. V1a and V1b are the voltage levels (with respect to some arbitrary reference) of the two input lines of the single-phase input to first matrix converter. Similarly, V2a and V2b are the voltage levels of the two input lines of the second matrix converter. Vo1 and Vo1' are the output line voltage levels of the first matrix converter and Vo2 and Vo2' are the output voltage levels of the second matrix converter. The actual realization of the configuration is shown in Fig. 2.



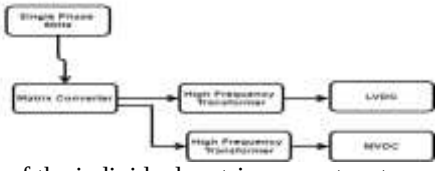


Fig. 3. configuration of the individual matrix converter stages

The cascaded output of the two matrix converters is derived as follows:

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- Switching Strategy for first matrix onverter

• Current starts to flow during the positive cycle, when switches, S1A and S4A will be kept ON . (state 1). (Ref Fig. 4 and 8)
• Current starts to flow during the positive cycle, when switches, S1B, and S4B will be kept ON. (state 2). (Ref Fig. 5 and 9)
• Current starts to flow during the positive cycle, when switches, S2A and S3A will be kept ON. (state 3). (Ref Fig. 6 and 10)
• Current starts to flow during the positive cycle, when switches, S2B and S3B will be kept ON. (state 4). (Ref Fig. 7 and 11)
The switching strategy is summarised in Table 1.

Table 1: Switching sequence for first matrix converter

Input Freque-ncy	Target output Frequenc y	Time Interva l	state	Switch modulate d	PWM	CPW M
50 Hz	5000 Hz	1	1	S_{1A}	S_{4A}	S_{2B}
		2	3	S_{2A}	S_{3A}	S_{1B}
		3	1	S_{1A}	S_{4A}	S_{2B}
		4	2	S_{1B}	S_{4B}	S_{3A}
		5	4	S_{2B}	S_{3B}	S_{4A}
		6	2	S_{1B}	S_{4B}	S_{3A}

The switching strategy for the second matrix converter can be derived on similar lines and is shown in Table 2.

Table 2:Switching sequence for second matrix converter

Input Frequ-ency	Target output Freque-ncy	Time Inter-val	state	Switch modula-ted	PWM	CPW M
50 Hz	5000 Hz	1	1	S_{1A1}	S_{4A1}	S_{2B1}
		2	3	S_{2A1}	S_{3A1}	S_{1B1}
		3	1	S_{1A1}	S_{4A1}	S_{2B1}
		4	2	S_{1B1}	S_{4B1}	S_{3A1}
		5	4	S_{2B1}	S_{3B1}	S_{4A1}
		6	2	S_{1B1}	S_{4B1}	S_{3A1}

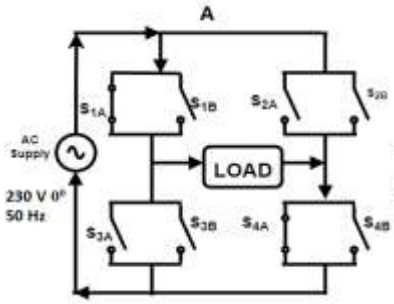

Fig. 4. State 1 positive cycle

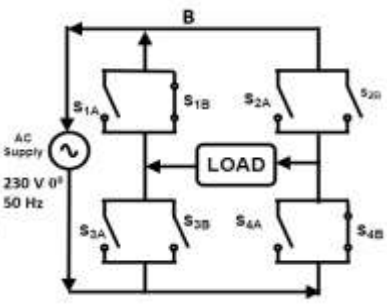

Fig. 5. State 2 negative cycle

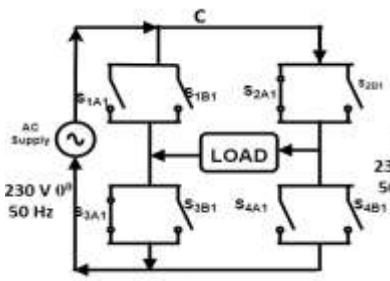

Fig. 6. State 3 positive cycle

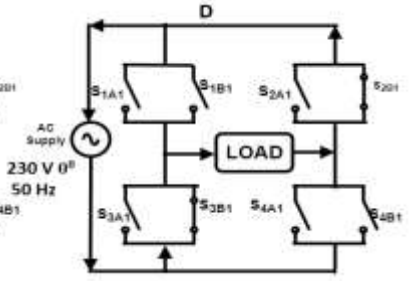

Fig. 7. State 4 negative cycle

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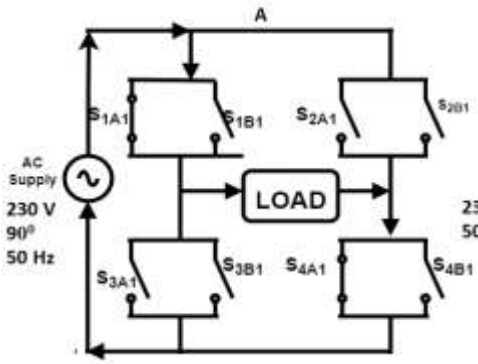

Fig. 8. State 1 positive cycle

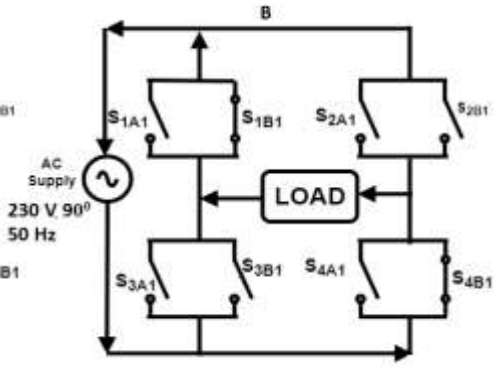

Fig. 9. State 2 negative cycle

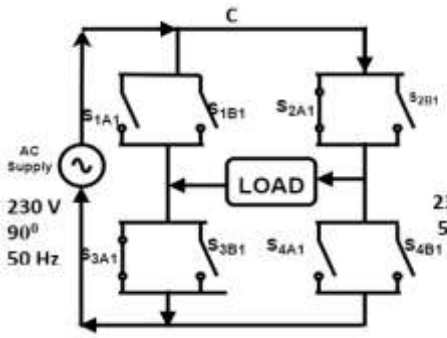

Fig. 10. State 3 positive cycle

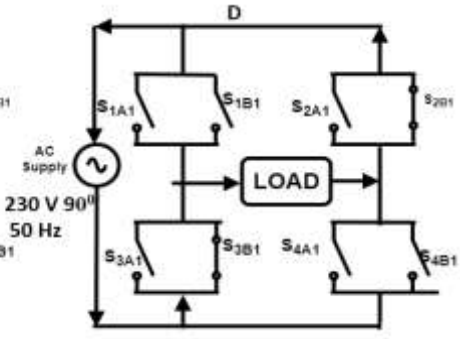

Fig. 11. State 4 negative cycle

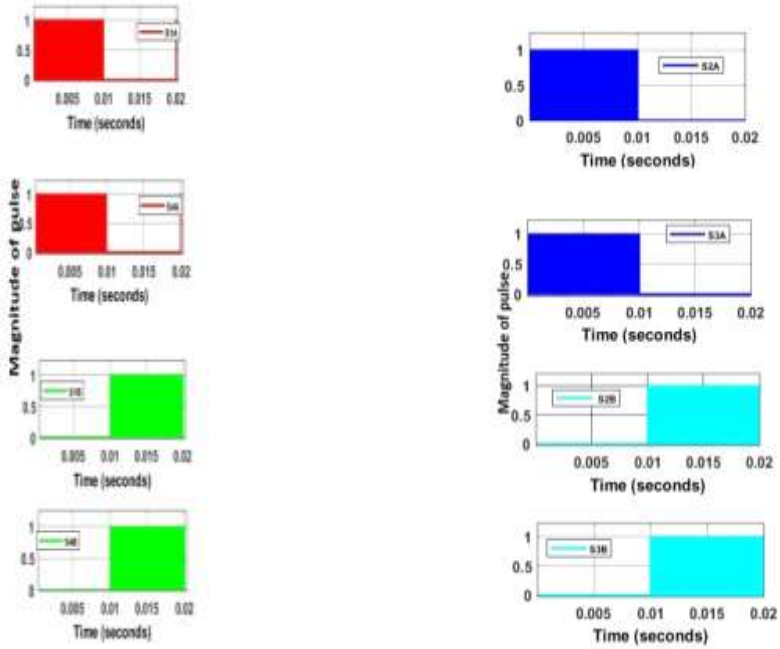

Fig. 12. Switching sequence in one cycle of input voltage

- **CONTROL STRATEGY**
- PI Controller for matrix converters

The matrix converter switching consists of symmetrically placed multiple pulses in each half cycle of the respective input voltages. The frequency of this pulse train is 5kHz. A simple PI controller is used to control the pulse widths of this train of pulses. The MVDC output voltage is

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compared with reference of 200 V and error signal is fed to the PI controller. The output of PI controller is suitable scaled and compared with a sawtooth carrier of 5 kHz frequency. The result in pulse width modulated train of pulses is given to various switches in the matrix converter stages as detailed in section. The Kp and KI parameters are obtained by Ziegler-Nichols method. Thus, cascaded output of the matrix converter essentially regulates the MVDC output to 200 V. The cascaded matrix converter output is also fed to the LVDC stage in parallel. Further there is buck converter stage in LVDC circuit which controls the LVDC level. SMC is used to regulate the LVDC to 12 V. Thus, MVDC is regulated at 200 V by controlling the matrix converter while the LVDC regulated at 12 V by controlling the buck converter.

- Sliding mode controller (SMC) for buck converter

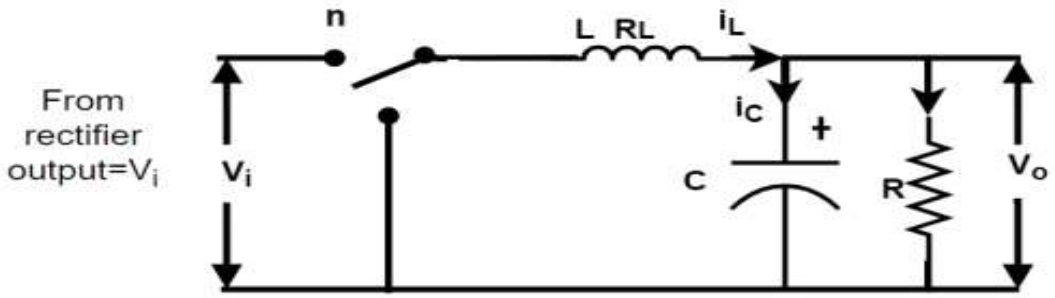

Fig. 13. The basic diagram of buck converter

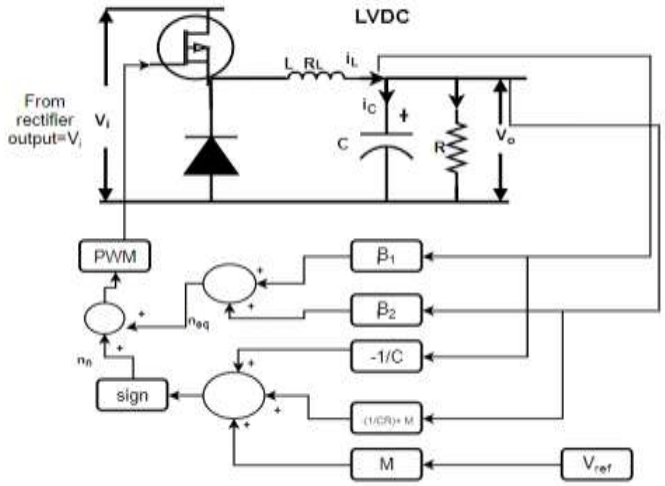

Fig. 14. SMC buck converter

The LVDC circuit along with its control Fig. 14 The derivation of the sliding mode surface obtained by applying KCL and KVL to the LVDC circuit is as follows:[11]
e : is the output voltage error, S-sliding surface, M-sliding mode coefficient [12]

The condition on the chosen sliding mode surface for reaching the origin is

Were,

IV. SIMULATION RESULTS

The typical simulation results of the PET obtained from MATLAB- Simulink are presented in this section. Fig. 16 shows the cascaded output of the two-matrix converter.

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Fig. 15. Input Voltage

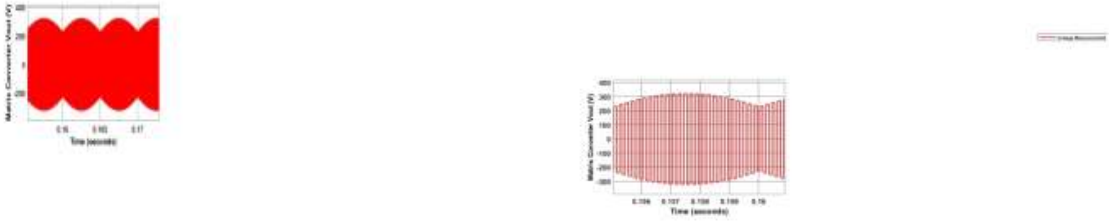
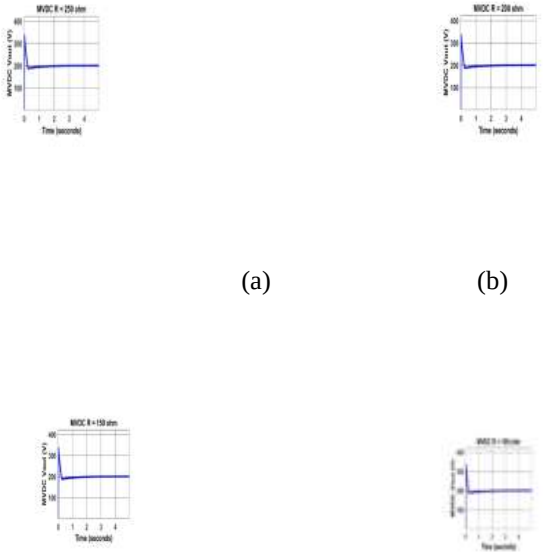


Fig. 16. Matrix converter output compression and expanded

The MVDC output for load resistance valves of 250 Ω, 200 Ω, 150 Ω and 100Ω are shown in Fig. 17 in a, b, c and d respectively. It is observed that the MVDC voltage tracks the reference of 200 V with zero steady state error for different loading conditions.



(a) (b)

(c) (d)

Fig. 17. MVDC output voltage different loading conditions with PI controllers for matrix and buck stages.

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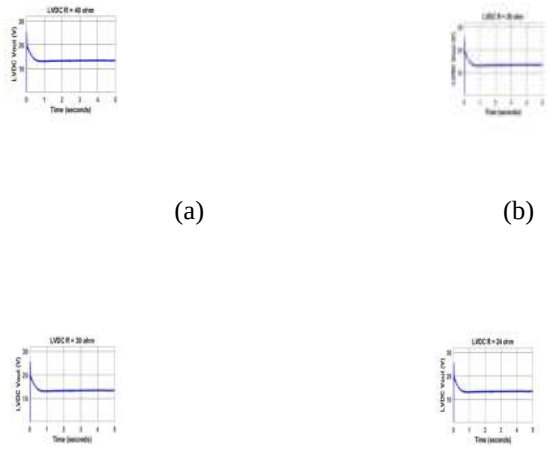
The LVDC voltage for different loads at LVDC port are presented in a, b, c and d for load resistance valve of 40 Ω, 36 Ω,30 Ω and 24 Ω respectively. Shown in Fig. 18.

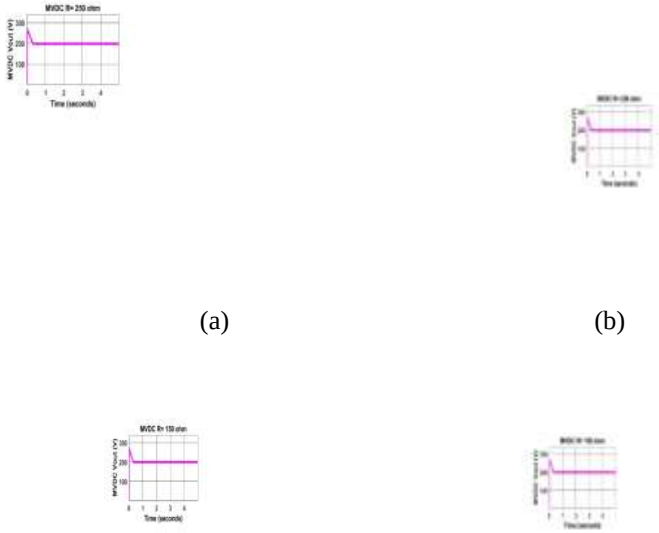


(a) (b)

(c) (d)

Fig. 18. LVDC output voltage different loading condition with PI controllers for matrix and buck stages.

The It is found from the above simulation results that the MVDC voltage and LVDC voltages are regulated with zero steady state error for different loading conditions at respective ports. It is also observed that there is decoupling between the two outputs for different loading conditions. It was also observed that the use of SMC for LVDC circuit improved the response of both MVDC and LVDC stages as is evident from Fig.17, Fig. 18, Fig. 19 and Fig. 20.



(a) (b)

(c) (d)

Fig. 19. MVDC output voltage different loading conditions with SMC for buck stage and PI controller for matrix conversion stages.

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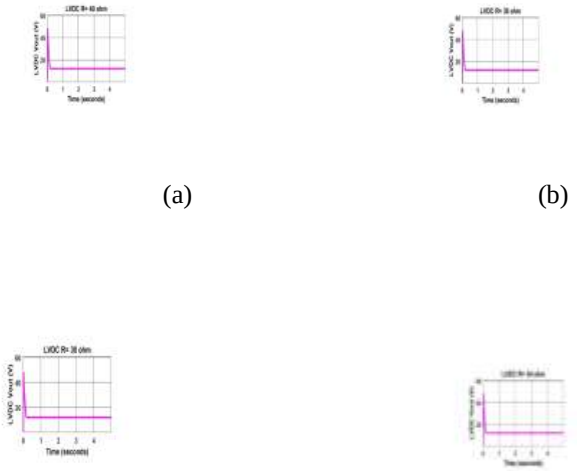

(a) (b)

(c) (d)

Fig. 20. LVDC output voltage different loading condition with SMC for buck stage and PI controller for matrix conversion stages.

- Rating

Parameters	Value
RMS of two single-phase voltage of AC grid	230 V
Rated voltage of MVDC port	200 V
Rated voltage of LVDC port	12 V
Filter inductance at MVDC side L	9 mH
Filter capacitance at MVDC side C	4000 F
Filter inductance at rectifier LVDC side L	1 mH
Filter capacitance at rectifier LVDC side C	4000
Filter capacitance at LVDC side C (SMC)	4700 F
Filter inductance at LVDC side L (SMC)	20 mH
Switching frequency of MC	5 kHz
Filter inductance at LVDC side L (PI)	3 mH
Filter capacitance at LVDC side C (PI)	2000 F
MFT turns ratio	4:1
Switching device	MOSFET IRFP450 25A/600V
Diode for LVDC	MUR3060
Diode for MCDC and Matrix-Converter	MUR3060

V. CONCLUSION

A novel power electronic transformer based on matrix converter, taking two phase-shifted, single phase, AC inputs of 230 V, 50 Hz and providing MVDC of 200 V and LVDC of 12 V, is conceived designed and extensively simulated in MATLAB-Simulink. Further, LVDC stage consists of medium frequency transformer followed by a buck converter. The hybrid control strategy - PI controller for the cascaded matrix converter and SMC for the buck converter is used. It is observed that MVDC and LVDC outputs are regulated at 200 V and 12 V respectively with zero steady state error for different loading conditions. Further, it is also observed that the hybrid mode of control improves the response as compared to a case where both

controllers are PI controllers. Use of matrix converters, instead of MMC, for the PET results in significant reduction in number of switches. The use of medium frequency carrier has resulted in reduction in transformer size. The simulation results agree with the analytical results. Such PETs will find application in hybrid distribution systems.

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